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Sun et al.

(54) THIN FILM TRANSISTOR ASSEMBLY, ARRAY SUBSTRATE METHOD OF MANUFACTURING THE SAME, AND DISPLAY DEVICE

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See application file for complete search history.

(56) References Cited

U.S. PATENT DOCUMENTS

2005/0258488 A1 11/2005 Chang et al.

2011/0101353 A1* 5/2011 Park H01L 29/78633 257/59

2013/0248870 A1 9/2013 Jung et al.

FOREIGN PATENT DOCUMENTS

CN 202473925 10/2012 CN 103018989 4/2013

(Continued)

OTHER PUBLICATIONS

International Search Report and Written Opinion from PCT Application Serial No. PCT/CN2015/073341, dated Jul. 17, 2015, 11 pages.

(Continued)

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(57) ABSTRACT

The present disclosure discloses a thin film transistor assembly, an array substrate and a method of manufacturing the same, and a display device including the array substrate. The array substrate includes a substrate; a plurality of thin film transistors formed on the substrate; and a plurality of light shielding layers, each of the light shielding layers being arranged between a source electrode and a drain electrode of the thin film transistor and configured to block light from the exterior from illuminating an active layer of the thin film transistor. The light shielding layer and the source electrode and the drain electrode of the thin film transistor are formed in the same layer on the substrate. As the light shielding layer, the source electrode and the drain electrode of the thin film transistor and a data line may be formed on the substrate (Continued)

